

## Introduction

Potential Induced Degradation (PID) is an undesirable property of some solar modules. The factors that enable PID (voltage, heat and humidity) exist on all photovoltaic (PV) systems, but the effect does not occur on all or even most PV systems. According to Dr. Peter Hacke of the National Renewable Energy Laboratory (NREL), "All c-Si [crystalline silicon] modules have elements of reversible and non-reversible [PID] mechanisms. The key is to understand the extent to which modules experience these mechanisms."

PID was first recognized in the 1970's, and has been studied since. The rapid growth in PV plant deployments, combined with dramatic reduction in module prices (and in some cases, module quality), has brought renewed interest in the phenomenon. And because the issue is highly technical, requiring at least some understanding of chemistry and physics, the renewed interest has been accompanied by substantial fear, uncertainty and doubt in the market today.

Although there are ways to mitigate PID, and mitigation is not always even necessary, the focus of this white paper is on its causes and effects in a PV power plant, and the status of tests for measuring PID. This discussion provides a summary of the extensive research Advanced Energy conducted to encourage and further education on the subject in the industry. Sources for this research are cited both in the text and in footnotes to assist anyone interested in learning more.

## CONTENTS

- Introduction  
*Page 1*
- Causes of PID  
*Page 1*
- Environmental Factors  
*Page 2*
- System Factors  
*Page 3*
- Module Factors  
*Page 4*
- Cell Factors  
*Page 4*
- Effects of PID  
*Page 5*
- Testing for PID  
*Page 6*
- Conclusion  
*Page 7*



## The Causes of PID

Potential Induced Degradation, as the designation implies, occurs when the module's voltage potential and leakage current drive ion mobility within the module between the semiconductor material and other elements of the module (e.g. glass, mount and frame), as shown in Figure 1, thus causing the module's power output capacity to degrade.

The ion mobility accelerates with humidity, temperature and voltage potential. Tests have revealed the relationship of mobility to temperature and humidity: "Planar contact with the panel surface also causes a capacitive coupling to the cells, resulting in a capacitive leakage current of varying strength." <sup>1</sup>

The PV system and environment interact to cause PID. The conditions necessary for the occurrence of PID involve (i) environmental factors, as well as factors involving (ii) the system, (iii) the module, and (iv) the cells.<sup>2,3</sup> "While the environment is set for each individual installation, it is possible to prevent PID by properly controlling only one of the factors (ii), (iii), or (iv)." <sup>4</sup> All four factors are discussed, in turn, below.

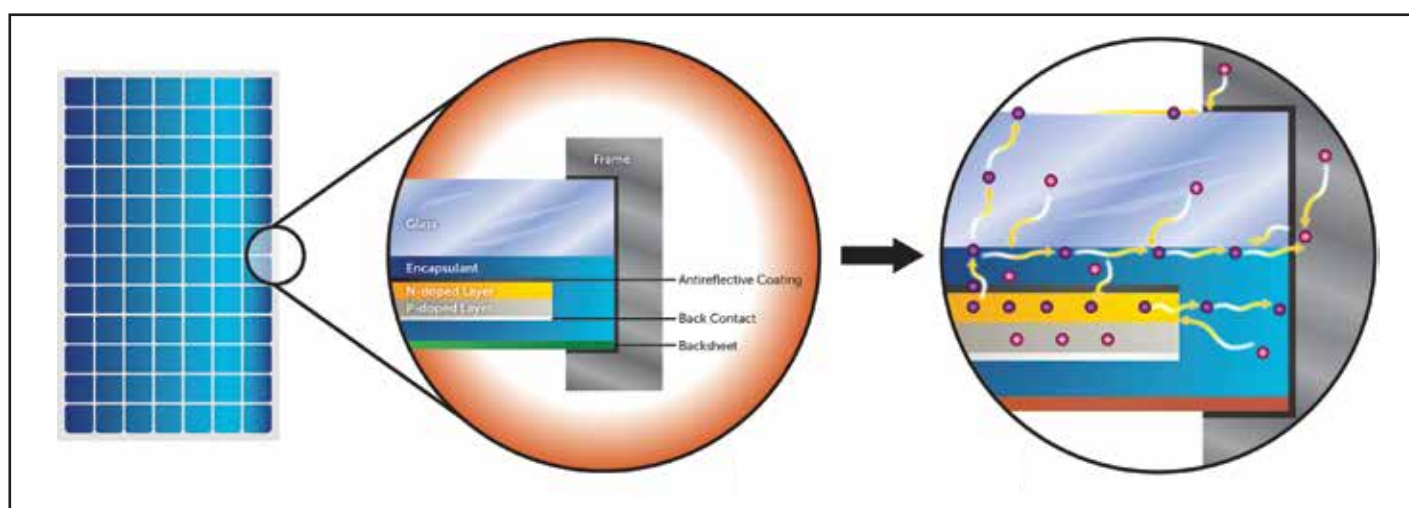


Figure 1 - Leakage current and voltage potential (negative potential shown) cause negative (-) (purple) ions to migrate away from the semiconductor, as positive (+) (pink) ions migrate toward the semiconductor from the glass and package, and the module's external environment.

## Environmental Factors

Because relative humidity and temperature are known to adversely affect PV plant performance in general, portions of both Underwriters Laboratories (UL) and International Electrotechnical Commission (IEC) module testing protocols involve damp heat, temperature cycling, and freeze/thaw cycling. These same environmental factors also affect PID, with the degradation being accelerated by increases in temperature and/or relative humidity.<sup>5</sup>

It is interesting to note that while high temperatures cause an increase in the degrading effect caused by PID, high temperatures have also been shown to facilitate regeneration of the modules to reduce PID.<sup>6</sup>

Because there is little or nothing an operator can do to change the PV plant's environment, PID is best understood and addressed by examining the system and its modules.

## System Factors

At the system level, the most significant impacts are the module's voltage potential and sign, which depend on both the module's position in the array and the system grounding topology. There are numerous considerations affecting system and inverter classification, but for the purposes of PID, the inverter(s) can be classified based on the voltage experienced by the arrays. As shown in Figure 2, four basic classifications are possible.

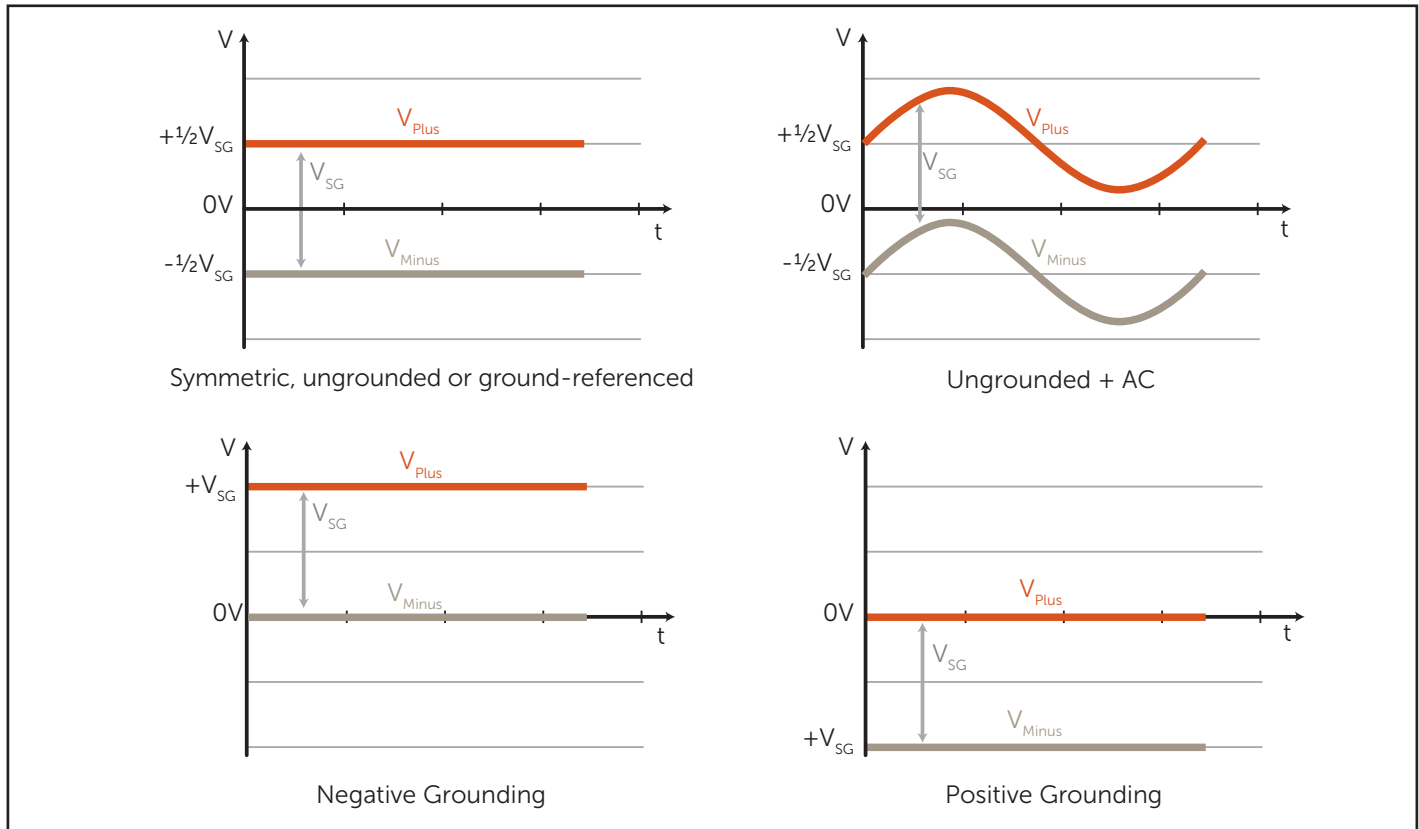


Figure 2 – Voltage potential depends on the grounding topology of the PV system, which can have these four basic classifications.

Figure 2 shows that the array voltage potential can vary based on the grounding topology. PID is most often associated with a negative voltage potential to ground, although issues arising from a positive reference to ground have been documented by SunPower.<sup>7</sup> Nevertheless, “[m]any years of experience with numerous systems provide a clear and reassuring answer: for panels with crystalline solar cells, there is no interrelationship between potential panel degradation and the inverter principle used.”<sup>[1]</sup>

Additional research has revealed that, “[a]n interpretation of the voltage dependency might be capacitive effects. Ionic migration caused by a certain electric force according to an applied voltage leads to a saturation of electric charge keeping all forces in thermodynamic equilibrium. These electrical charges influence the semiconducting properties... [r]egardless of the voltage level itself the modules' degradation processes stabilize on certain levels which seem to be characteristic for each module type.”<sup>8</sup>

Further research will be needed to understand the impact of higher array voltages on PID. The U.S. is beginning to adopt 1000V arrays, and throughout the industry the use of 1500V and even 2000V arrays is being considered as a means of reducing system costs in large commercial and utility-scale PV plants. Resistance to PID will become increasingly critical as array voltages increase. One theory, for example, postulates that in arrays of 1500V or more, a high positive potential is capable of causing new failure mechanisms.<sup>9</sup>

## Module Factors

The choice of glass, encapsulation, and diffusion barriers have all been shown to have an impact on PID. For the front glass, several studies have shown sodium to exhibit a causative factor.

According to one study, “[a]n ingredient contained in soda-lime glass but not in Quartz glass is required for the effect to occur... It was suggested that this species might be sodium. [5] While sodium is the prime suspect due to its availability and high mobility, “aluminum, magnesium, and calcium are present in smaller concentration in soda-lime glass but not in Quartz glass and might contribute to the difference.” [4]

The various means for encapsulating modules have significantly different properties, and these have been shown to have an equally significant effect on PID: “EVA [ethylene vinyl acetate] appears to also play a vital role in PID since all the different substitutes... were able to prevent PID. It was proposed that this finding might be linked to differences in conductivity. [3] Furthermore, acetic acid contained in EVA in conjunction with moisture might be responsible for dissolution of metal ions at the glass interface, known as ‘glass corrosion’. The results... indicate that PID is associated with a transport process through the interface between glass and EVA as well as through the interface between EVA and the cell surface.” [4]

Another test indicated that module samples laminated with polyvinyl butyral (PVB) show the highest susceptibility to PID. [8] PVB has a very low resistance to moisture intrusion, and more moisture increases conductivity. Other encapsulants that have superior moisture permeability properties compared with EVA have been shown to reduce susceptibility to PID: “The use of alternative materials is also recommended based on the fact that leakage currents in the module can, in principle, be curtailed by using an encapsulation material that is impermeable to charge carriers.” [6]

Using silicon dioxide as a sodium diffusion barrier between the glass and the electrically active portions of the semiconductor has been shown to work fairly well at preventing PID, but such a barrier is not immune to “pin-hole” leaks. Additionally, laser-ablation of the front contact for thin film applications can leave gaps in the barrier layer, which can become problematic without post-processing steps to fill these gaps.

## Cell Factors

An anti-reflective coating (ARC) increases the capture of light and, therefore, increases module power conversion. But research has shown ARC properties to be a causative factor in PID: “ARC is another prerequisite for the PID process. This is in agreement with the reported dependency of PID on ARC properties. [2][3] It was recently found from SIMS [secondary ion mass spectrometry] measurements that sodium originating from the glass can be readily found in the top layers of the cell.” [4] 10



## The Effects of PID

As shown in Figure 3, the reduction in shunt resistance ( $R_{sh}$ ) caused by PID reduces both the module's maximum power point (MPP) and its open circuit voltage ( $V_{oc}$ ).<sup>[4]</sup> TÜV Rheinland Group identifies the problem using three factors: yield reductions; power and voltage losses; and infrared (IR) imaging.<sup>[6]</sup>

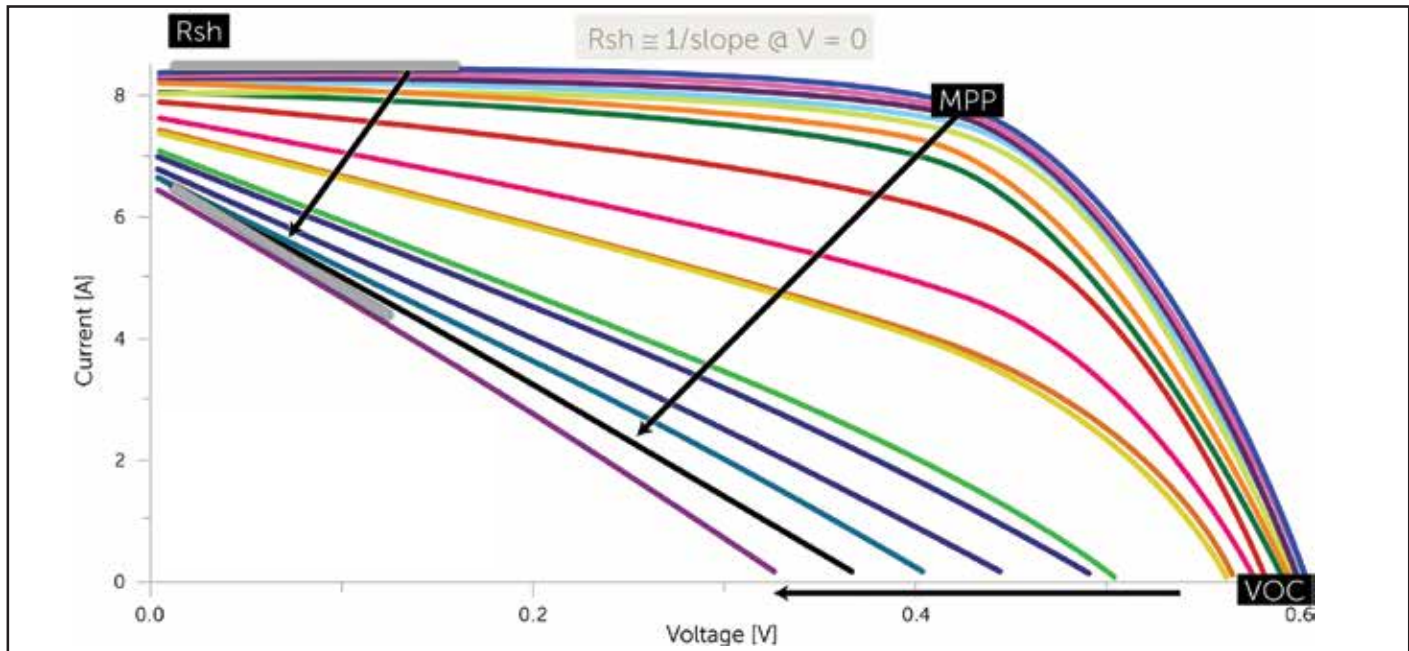


Figure 3 – As shown here by the reductions in shunt resistance ( $R_{sh}$ ), maximum power point (MPP) and open circuit voltage, PID can significantly reduce yield in PV plants. [Source: Schuetze, et al, Laboratory Study of Potential Induced Degradation of Silicon Photovoltaic Modules]

Unexplainable yield losses can be a sign of PID. Because measuring  $R_{sh}$ , MPP and IR signatures require expensive equipment, the easiest way to detect PID in the field is to use an ordinary voltmeter to measure module-level  $V_{oc}$ . While the shape of the diode curve shown in Figure 3 cannot be inferred by  $V_{oc}$  alone, the extent of PID can be revealed by plotting  $V_{oc}$  measurements by string position, or comparing the  $V_{oc}$  measurements from opposite ends of the array.

The PID effect can be either irreversible or reversible, depending on the cause. Obviously an irreversible effect is far more serious, requiring immediate detection and mitigation. Irreversible PID is typically caused by electrochemical reactions that leads to electro-corrosion and/or film delamination in the modules. These irreversible characteristics have been documented primarily in thin film technologies, and are therefore not a focus of c-Si panel manufacturers.

The reversible form of PID, also known as “Surface Polarization” or the “Polarization Effect,” was discovered by SunPower in 2005.<sup>[7]</sup> According to SunPower’s announcement of the discovery, “[t]his new effect, called ‘surface polarization,’ creates the non-destructive and reversible accumulation of static charge on the surface of high-efficiency solar cells.” The Polarization Effect has since been studied and documented by Solon<sup>[2]</sup> and many others and is generally associated with c-Si modules.

As a result of these studies, the specific effect occurring between the glass and the semiconductor is now well understood: “Models are based on the fact that mobile sodium ions can diffuse from the front glass to the cell surface due to a force caused by potential induced stress. The velocity of the positive charged ions are mainly influenced by the encapsulate material, the temperature, the humidity and the applied voltage.”<sup>[8]</sup>

The specific mechanisms occurring once sodium reaches the semiconductor are not as well understood, and several different theories have been proposed: “On the one hand the charged ions concentrate on the surface of the layer building up an electric field leading to an anti-passivating effect resulting in an increasing surface recombination rate. On the other hand the sodium may diffuse into the bulk and act as a donator atom. This leads to a rising concentration of sodium ions in the emitter, so the negative doping will be neutralized, the p-n-junction will be diminished, [and] so [is] the photovoltaic effect of the cell.”<sup>[8]</sup>

Regardless of the specific mechanisms, extensive testing has demonstrated the ability to reverse the polarization effect, and thereby fully restore the power output of the modules. One such test was conducted at Arizona State University. [9] Another test, the results of which are shown in Figure 4, found that reversing polarity fully mitigates the polarization effect. [2]

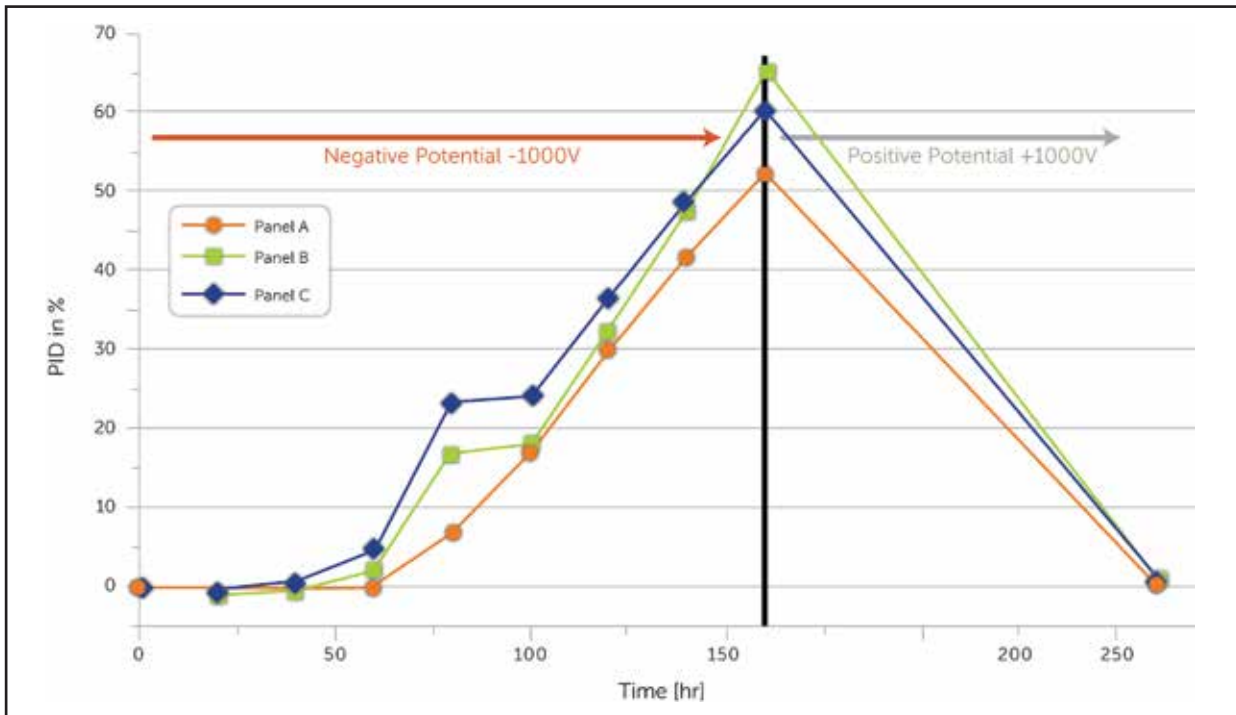


Figure 4 – The Polarization Effect on c-Si modules can be fully mitigated by reversing the potential voltage applied. [Source: S. Pingel, et al, Potential Induced Degradation of Solar Cells and Panels]

## Testing for PID

Testing modules for susceptibility to PID is now important in any large-scale PV project, and is often needed to obtain financing. Testing will also determine if the mechanism causing PID is reversible, which determines whether mitigating measures are required and what measures are appropriate.

A full list of testing agencies and the modules tested to date is provided in the November 2012 issue of *Photon International Magazine*. [6] Many testing organizations currently offer PID testing, including:

- NREL (<http://www.nrel.gov/>)
- Fraunhofer (<http://www.fraunhofer.org/>)
- Intertek (<http://www.intertek.com/>)
- CFV Solar Test Laboratory ([www.cfv-solar.com](http://www.cfv-solar.com))
- PV Evolution Labs ([www.pvel.com](http://www.pvel.com))
- TÜV Rheinland PTL ([www.tuvptl.com](http://www.tuvptl.com))
- TÜV SÜD America ([www.tuv-america.com/services/photovoltaics.cfm](http://www.tuv-america.com/services/photovoltaics.cfm))
- Pearl Laboratories (<http://www.pearllaboratories.com/>)
- PI Berlin (<http://www.pi-berlin.com/>)

A test standard is being developed by a consortium of industry experts led by Dr. Peter Hacke of NREL. The team is expecting to have the Final Draft International Standard (FDIS) for IEC 62804 in 2014. The standard is expected to be adopted by testing organizations, and many are already using its preliminary provisions. The IEC 62804 standard will prescribe a very specific test procedure and the basic conditions for conducting the test, including:

- Module-rated system voltage and polarities
- Chamber air temperature  $60^{\circ}\text{C} \pm 2^{\circ}\text{C}$
- Chamber relative humidity  $85\% \pm 5\%$
- Test duration of 96 hours at above stated temperature and relative humidity with applied stated voltage

Under the IEC 62804 standard, modules will be deemed to be PID-resistant if:

- Power loss is less than 5%
- There is no evidence of any major defect as defined in IEC 61215 clauses 10.1, 10.2, 10.7, and 10.15.

## Conclusion

Potential Induced Degradation can have profound adverse impact on the financing and operating of PV plants. While the entire PV system interacts to cause PID, the failure mode occurs in the modules. Fortunately PID does not occur in all modules, and tests are available to determine whether modules are susceptible or resistant to the effect. Many module manufacturers have taken steps to produce PID resistant modules. And for existing c-Si modules that do experience PID, the effect is usually reversible with cost-effective mitigation measures.

Because mitigating PID in the PV plant can increase initial system costs, a judicious choice of resistant modules and other preventative efforts, within the constraints of each individual system, may be warranted. But it is also possible, of course, to intentionally design a new PV plant with modules susceptible to PID if the savings from using such modules is greater than the mitigation measures required. Refer to the *Mitigating Panel Polarization* application note for options using Advanced Energy inverters.

The best solution for the industry long-term is to minimize or eliminate PID by making design changes at the system, module and/or cell levels. Until then, it will remain important for operators to overcome any fear, uncertainty, and doubt by becoming more knowledgeable about PID, and hopefully the information and references provided here help achieve that objective.

<sup>1</sup> Heribert Schmidt and Bruno Burger, *Interactions between Solar Panels and Inverters*, Fraunhofer-Institut für Solare Energiesysteme (ISE), December 2010

<sup>2</sup> S. Pingel, et al, *Potential Induced Degradation of Solar Cells and Panels*, 35TH IEEE PVSC, 2010

<sup>3</sup> J. Berghold, et al, *Potential Induced Degradation of Solar Cells and Panels*, 25TH EUPVSEC, 2010, pp 3753-3759

<sup>4</sup> Schuetze, et al, *Laboratory Study of Potential Induced Degradation of Silicon Photovoltaic Modules*, Q-Cells SE, Sonnenallee 17-21, 06766 Bitterfeld-Wolfen

<sup>5</sup> P. Hacke, et al, *System Voltage Potential-Induced Degradation Mechanisms in PV Modules and Methods for Test*, NREL, 37TH IEEE Photovoltaic Specialists Conference (PVSC 37), Seattle, Washington, 19-24 June 2011

<sup>6</sup> Rutschman, Ines, *Power Losses below the Surface*, Photon International Magazine, November 2012, pp 130-137

<sup>7</sup> R. Swanson, et al, *The Surface Polarization Effect in High-Efficiency Silicon Solar Cells*, 2005, SunPower Corporation

<sup>8</sup> S Koch, et al, *Polarization Effects and Tests for Crystalline Silicon Cells*, 26TH European Photovoltaic Solar Energy Conference and Exhibition, 5-8 September 2011, Hamburg, Germany

<sup>9</sup> Ebniali, Faraz, *Potential Induced Degradation of Photovoltaic Modules: Influence of Temperature and Surface Conductivity*, Arizona State University, April 2012

<sup>10</sup> P. Hacke, et al, *Characterization of Multicrystalline Silicon Modules with System Bias Voltage Applied in Damp Heat*, 25TH EUPVSEC, 2010, pp 3760-3765



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